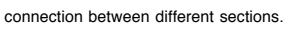
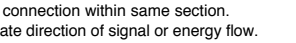
Facit 1123 Calculator

Contents

Notes

- IC numbering: IC*brc* where *b*=board, *r*=row, *c*=column. Board is 1,2 or 3 starting from the top. Row and column are counted from top left corner of board while holding board with parts up and connector on the right. See Physical Layout page.
- Gate symbols and signal names are presented in accordance with:
  logic 0 = GND
  logic 1 = Vcc
- The symol  denotes a physical connector pin, where *b* =1 to 3 for the PC board connectors starting from the top, K for the keyboard connector and R for the test/remote connector underneath the chassis, and *pp*=pin. Solid black end is the male side of the connector. White end is the female side of the connector.
-  connection between different sections.
   connection within same section.
  Arrows indicate direction of signal or energy flow.
- The symbol  denotes Vcc.
- Capacitance in microfarads unless otherwise indicated.
- These drawings based on unit with Serial No.: 302.500.
- Drawn by bhilpert. See www.cs.ubc.ca/~hilpert/eec for additional information.

Change Log

- July 1996: Initial creation.
- 31 Oct 2004: Manual control notes added. N4 and N5 renamed to NK and NR.

OP-Cycles and Manual Control of Operations

A switch can be plugged into the remote connector (NR) to provide the ability to single-step through the major state cycles of an operation. See the Keyboard & OP page for wiring of the switch.

An OP-cycle is a full number cycle during which processing occurs and is indicated by the OP signal. Major state transitions occur at the end of an OP-cycle. Simple user operations such as numeral entry generate a single OP-cycle without sending P0 to 0. More complex operations requiring multiple number cyclesgenerate a first OP-cycle and send P0 to 0. Multiple OP-cycles are subsequently generated until the operation is complete, at which time P0 returns to 1.

Enabling the MANUAL switch disables the automatic generation of OP-cycles for multi-cycle operations. In this mode, once a multi-cycle operation has been initiated, each press of the CLE key generates a single OP-cycle, so the operation can be stepped through one OP-cycle at a time.

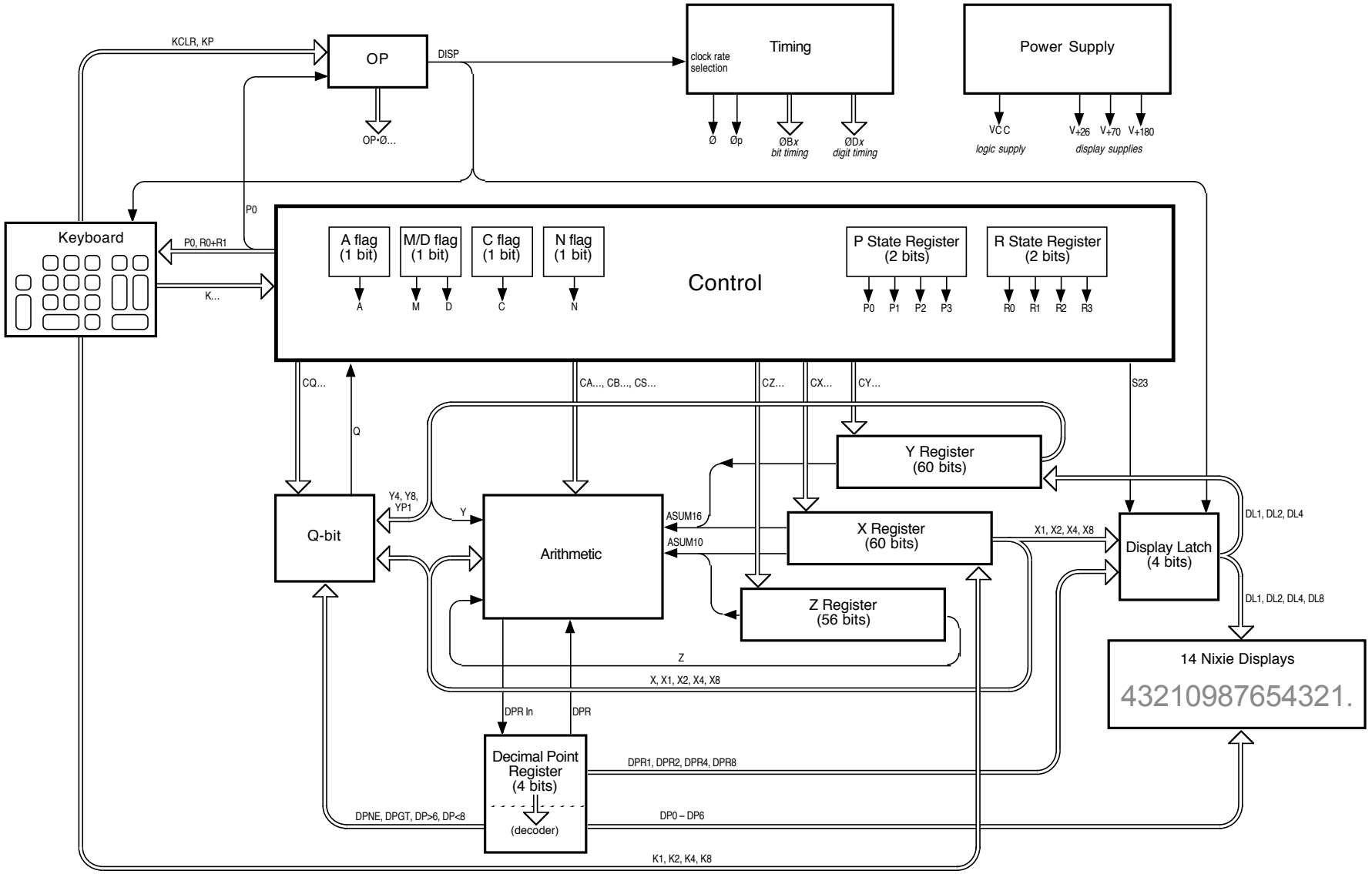
Signal Names

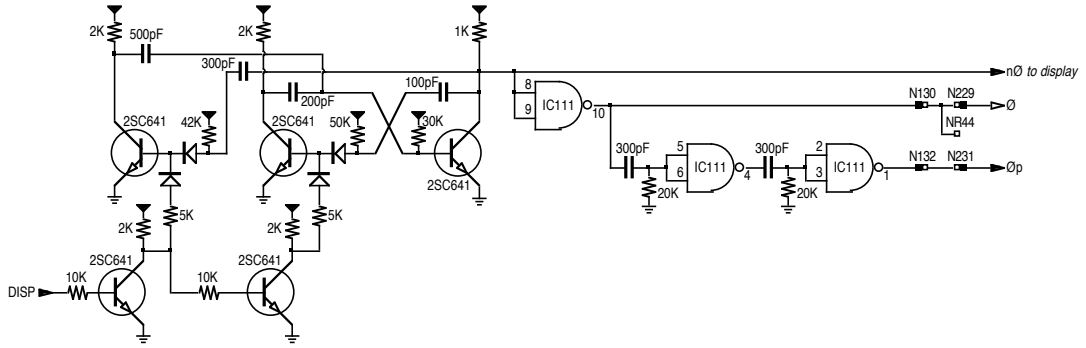
Section	Signal	Description
Timing	Ø…	Master timing.
	Ø	Master clock from which all timing is derived. This is the basic bit rate.
	ØB…	Bit timing.
	ØD0…ØD15	Digit Timing. 16 digit intervals, ØD2–ØD15 are the displayed digit time periods; Registers do not cycle during ØD0.
Keyboard	K…	various (unlatched) indications from the keyboard.
	A	1=Add, 0=subtract.
	C	1=calculation is multiply or divide, 0=add or subtract.
	M	1=Multiply
	D	1=Divide
	N	1=Normal mode, 0=use the Z register, also associated with the decimal point.
OP	OP…	Operation cycle.
Control	P0	state 0 of the 2-bit P state register: 1=idle, 0=calculating.
	P1 – P3	the other 3 states of the P register indicating some aspect of calculation.
	R0 – R3	the 4 states of the 2-bit R state register.
	S<*p*><*r*>	shorthand for states of the P and R register: S<*p*><*r*> = P<*p*> • R<*r*> .
	DISP	1=displaying, 0=calculating , same as P0 but with additional control from connector N5.
	CY…	Outputs from control to the Y register.
	CX…	" the X register.
	CZ…	" the Z register.
	CA…	" select the source for the A input of arithmetic.
	CB…	" select the source for the B input of arithmetic.
	CS…	" select the arithmetic function.
	CD…	" the decimal point register.
	CQ…	" the Q flag.
X Register	X…	The operand being displayed.
	X1,X2,X4,X8	BCD numerals on their way to the display.
Y Register	Y…	The second operand.
	Y	
	YP1	
Z Register	Z	The user memory.
DP Register	DP…	The decimal point register.
Arithmetic	ASUM16	The raw digit sum from the serial adder, base 16.
	ASUM10	The normalized digit sum after correcting for values between 10 and 15 inclusive.
Q Flag	Q	The 1-bit Q flag for catching data conditions.
Display Latch	DL…	Latch for numerals during the digit display interval, also used for transferring from the DP register to the Y register.

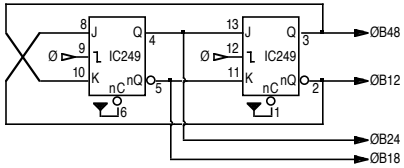
- A lowercase "n" in a symbol name indicates the logical NOT operation.
- The character " • " in a symbol name indicates the logical AND operation.
- The character "+" in a symbol name indicates the logical OR operation.

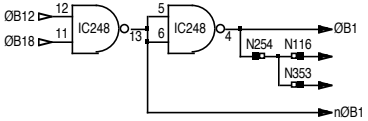
Algorithm Notes

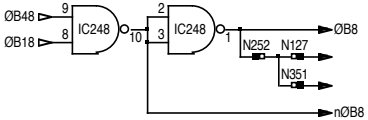
- During multiply and divide, a hex 'F' is placed after the LSD of one of the operands. The operand is shifted up to the upper end of the register and the F is used to indicate where arithmetic will begin during the number cycle.
- During multiply and divide, the uppermost digit of the Y register is used as a digit counter to limit the multiply/divide loop.

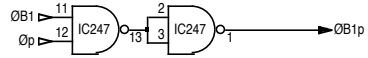

KCLR, KP
OP
DISP
OP•Ø...
Timing
clock rate selection
Ø
Øp
ØBx
bit timing
ØDx
digit timing
Power Supply
VCC
logic supply
V+26
V+70
V+180
display supplies
Keyboard
P0
P0, R0+R1
K...
A flag (1 bit)
M/D flag (1 bit)
C flag (1 bit)
N flag (1 bit)
A
M
D
C
N
Control
P State Register (2 bits)
P0
P1
P2
P3
R State Register (2 bits)
R0
R1
R2
R3
CQ...
Q
CA..., CB..., CS...
CZ...
CX...
CY...
S23
Y Register (60 bits)
Q-bit
Y4, Y8, YP1
Y
Arithmetic
ASUM16
ASUM10
X Register (60 bits)
X1, X2, X4, X8
Display Latch (4 bits)
DL1, DL2, DL4
DL1, DL2, DL4, DL8
Z Register (56 bits)
Z
X, X1, X2, X4, X8
14 Nixie Displays
43210987654321.
DPR In
DPR
Decimal Point Register (4 bits)
(decoder)
DPR1, DPR2, DPR4, DPR8
DPNE, DPGT, DP>6, DP<8
DP0 – DP6
K1, K2, K4, K8

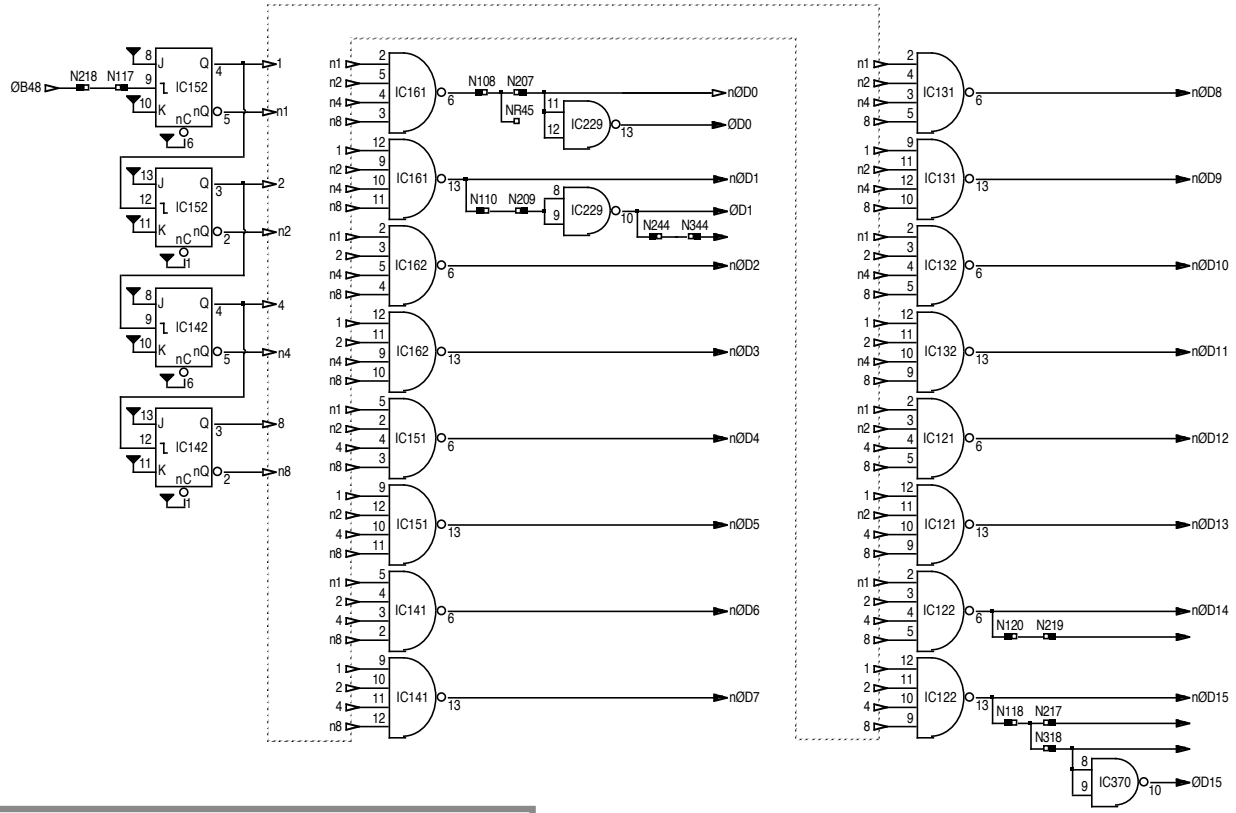


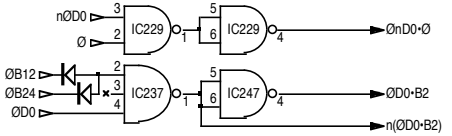












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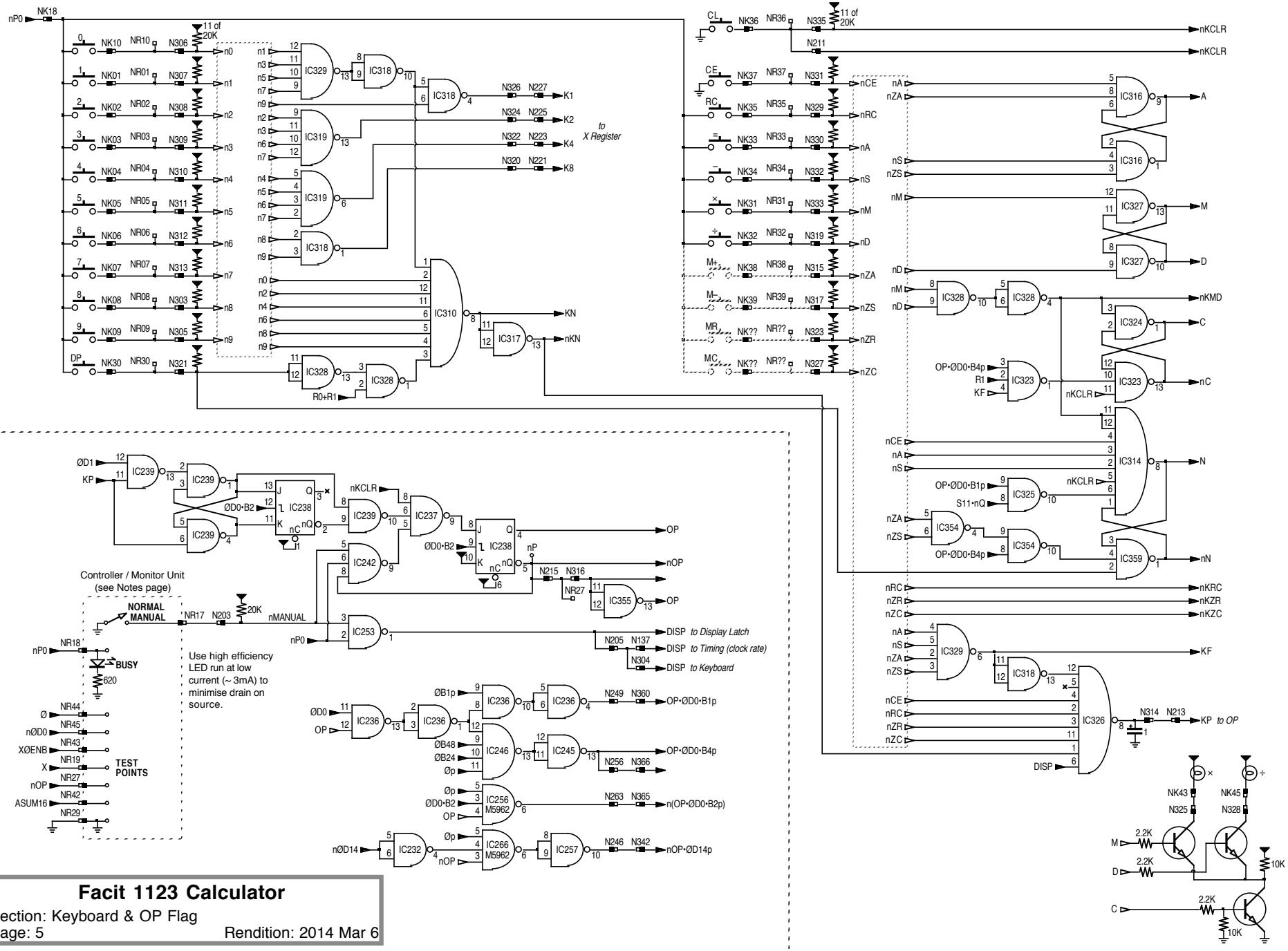
Section: Timing

Rendition: 2014 Mar 6



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Section: Keyboard & OP Flag

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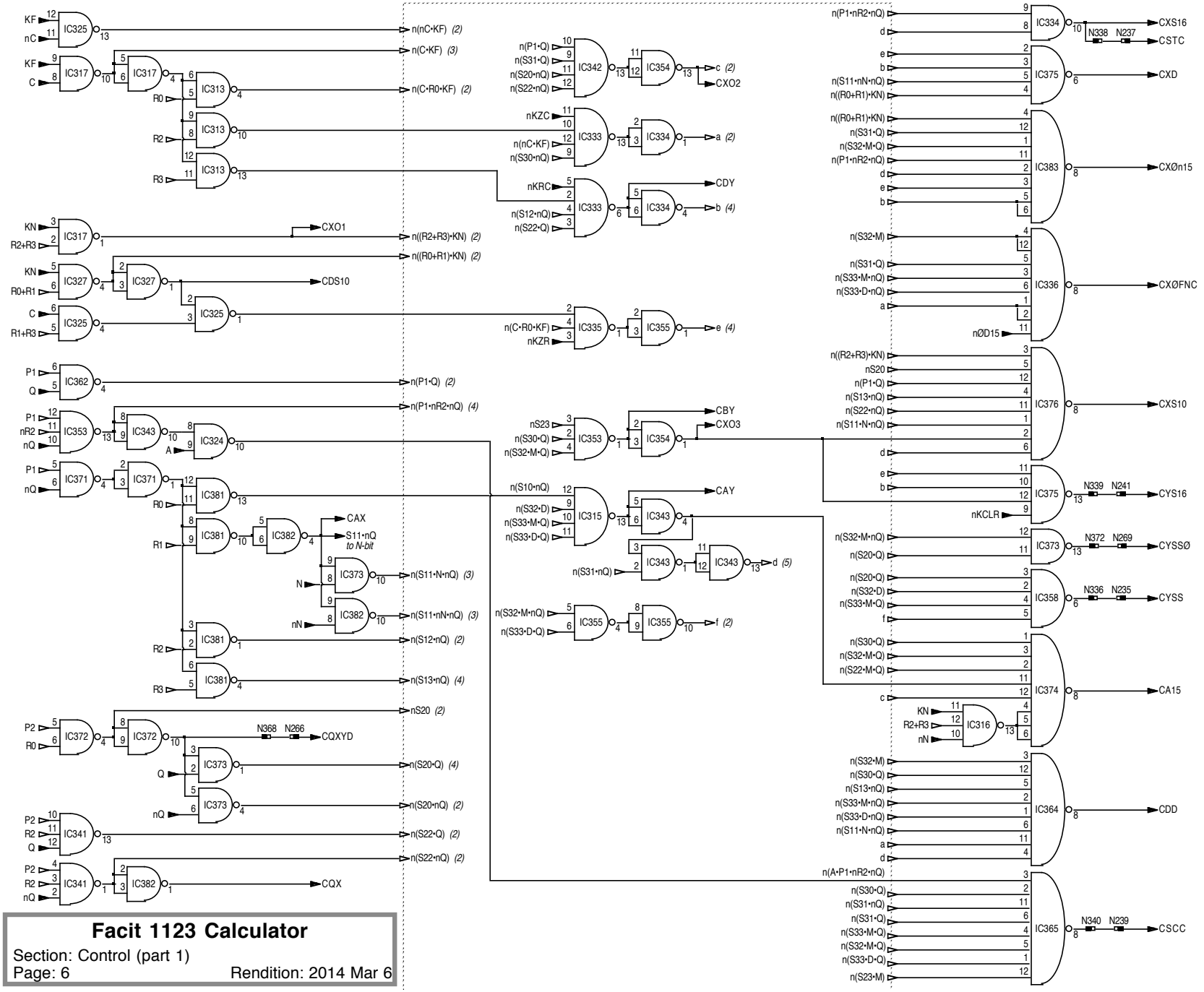
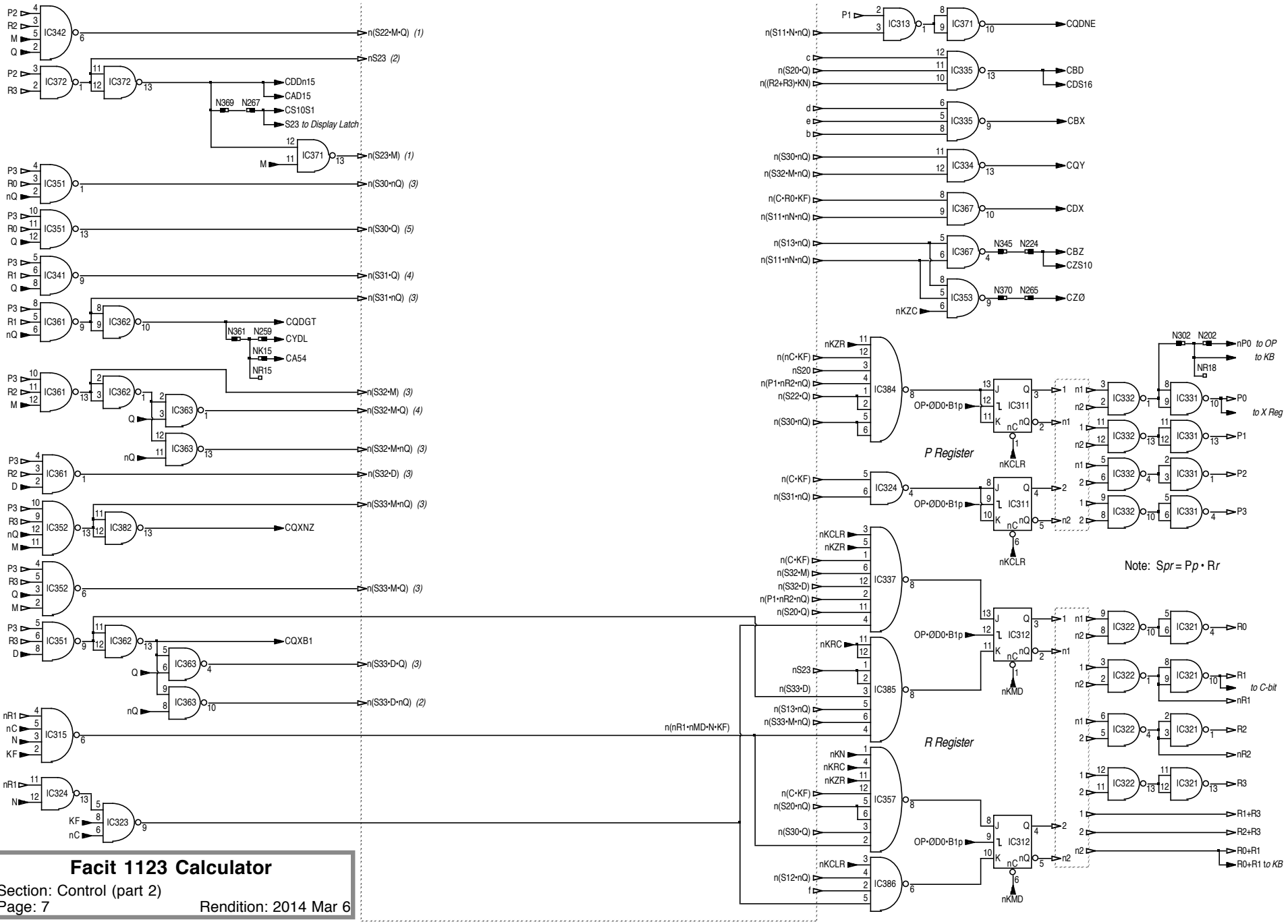


Facit 1123 Calculator

Section: Control (part 1)

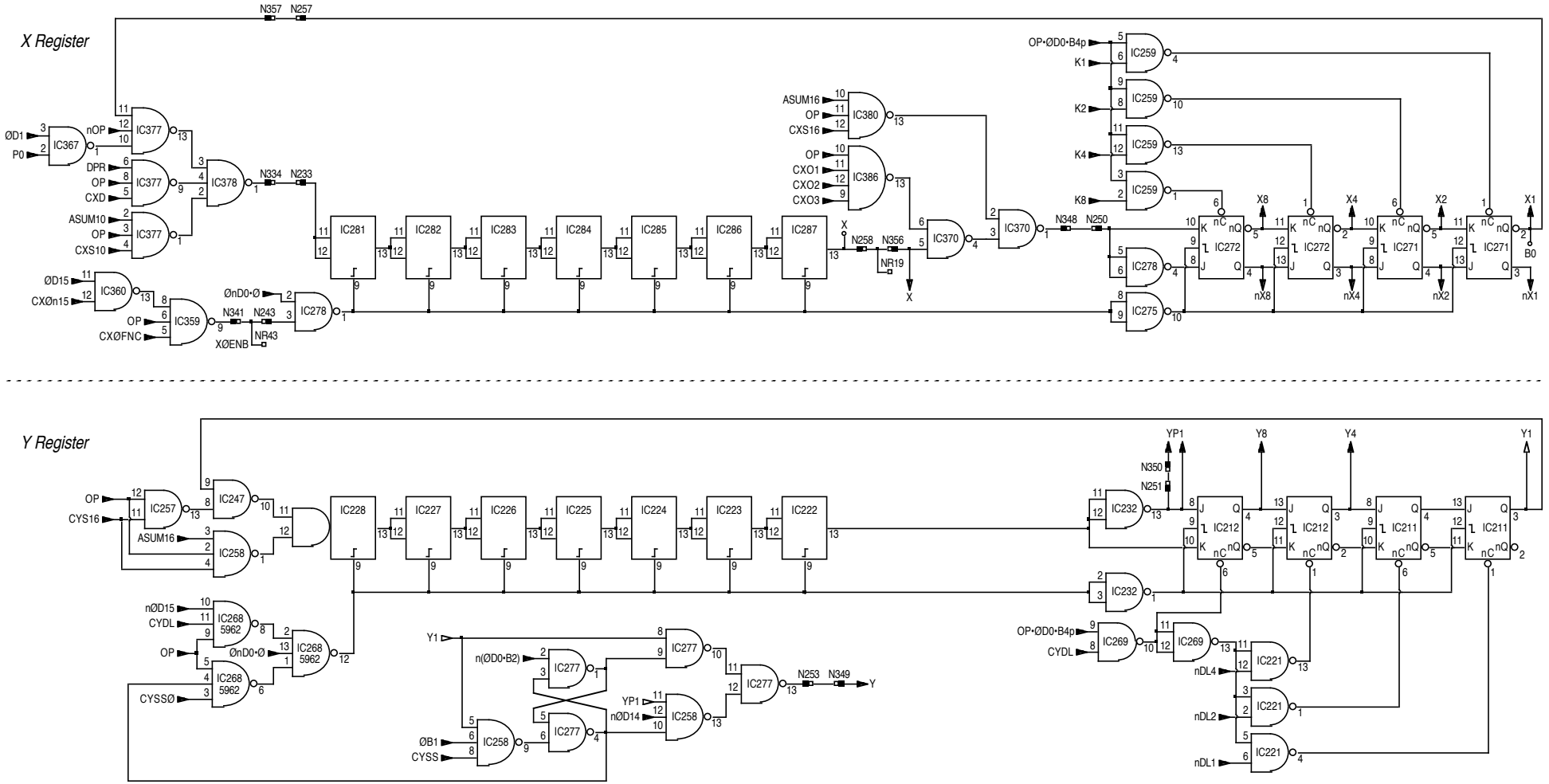
Page: 6 Rendition: 2014 Mar 6



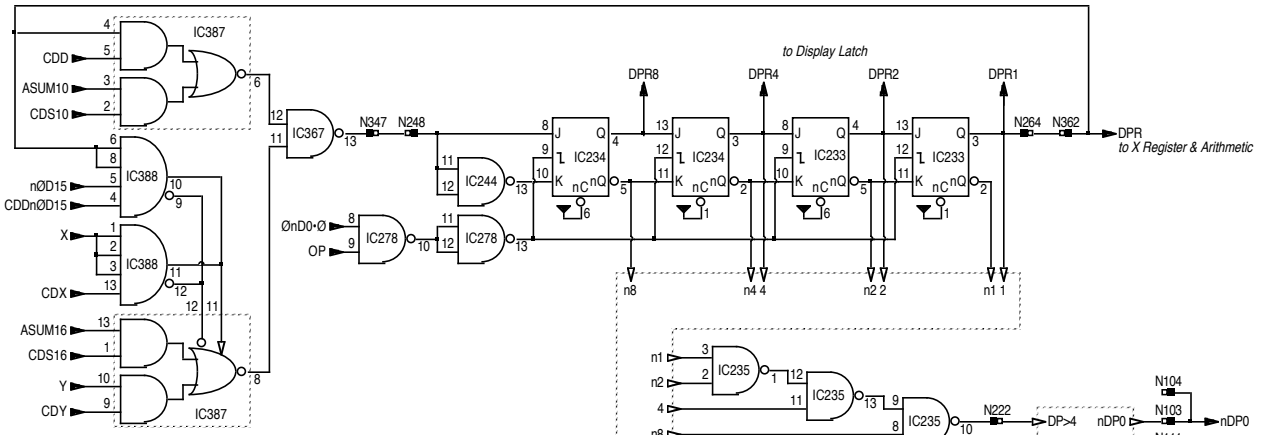
Facit 1123 Calculator

Section: Control (part 2)

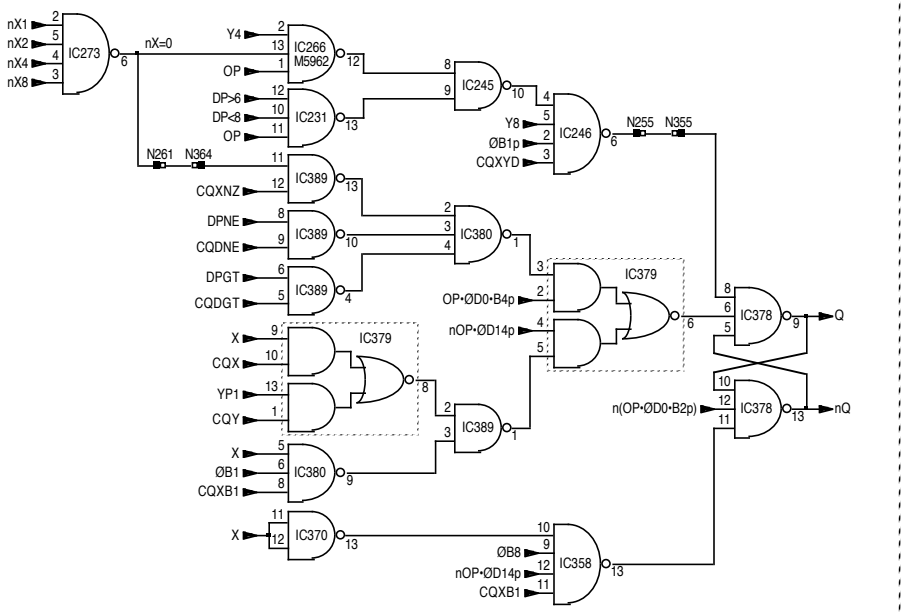
Page: 7 Rendition: 2014 Mar 6

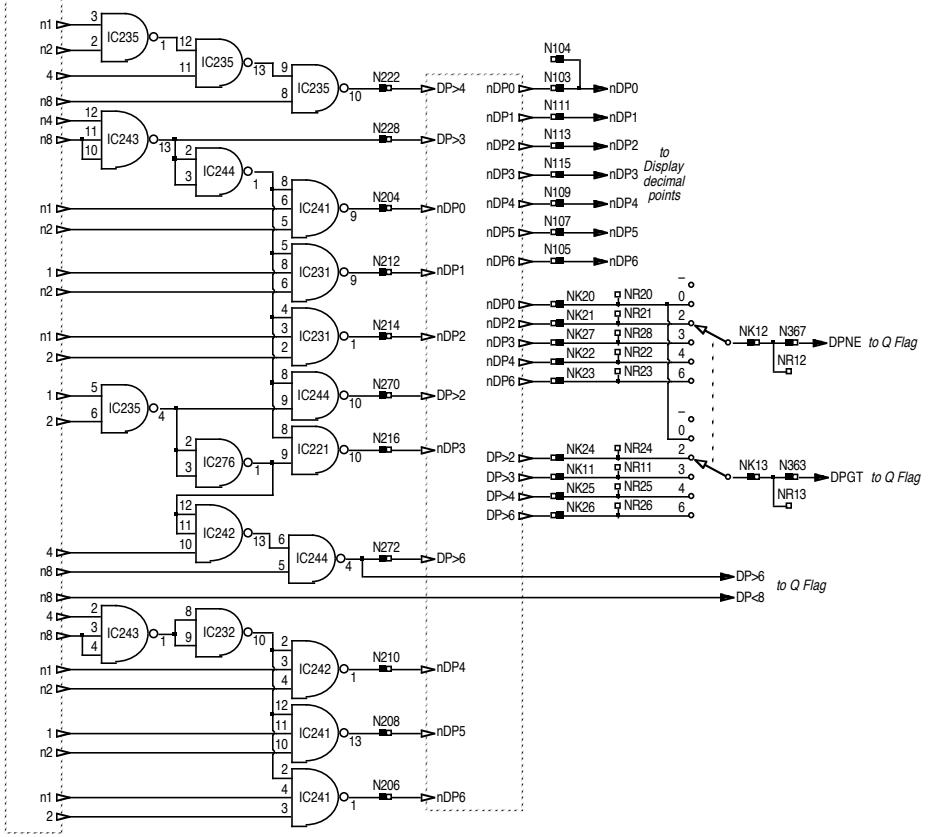

X Register
Y Register
Z Register
IC367
IC377
IC378
IC359
IC360
IC278
IC281
IC282
IC283
IC284
IC285
IC286
IC287
IC380
IC386
IC370
IC259
IC272
IC271
IC275
IC247
IC257
IC258
IC228
IC227
IC226
IC225
IC224
IC223
IC222
IC232
IC212
IC211
IC269
IC221
IC268 5962
IC277
IC213
IC214
IC215
IC216
IC217
IC218
IC219
IC237
ØD1
P0
nOP
DPR
OP
CXD
ASUM10
CXS10
ØD15
CXØn15
CXØFNC
XØENB
ØnD0•Ø
N357
N257
N334
N233
N341
N243
NR43
ASUM16
CXS16
CXO1
CXO2
CXO3
N258
N356
NR19
N348
N250
OP•ØD0•B4p
K1
K2
K4
K8
X8
X4
X2
X1
B0
nX8
nX4
nX2
nX1
N350
N251
YP1
Y8
Y4
Y1
CYS16
CYDL
nØD15
CYSSØ
n(ØD0•B2)
nØD14
ØB1
CYSS
N253
N349
Y
nDL4
nDL2
nDL1
CZS10
CZØ
Z

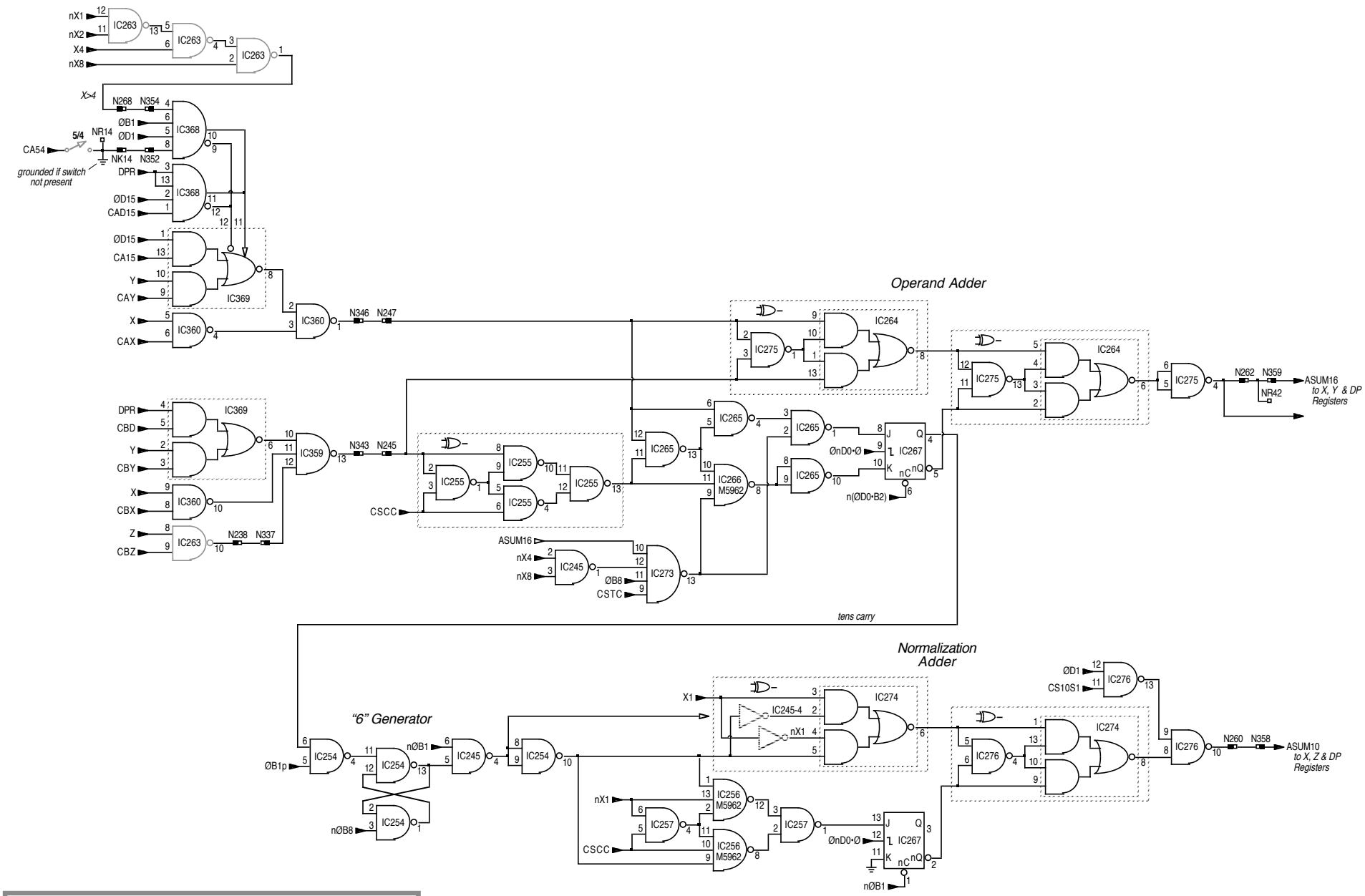
Decimal Point Register



Q Flag







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Section: Arithmetic
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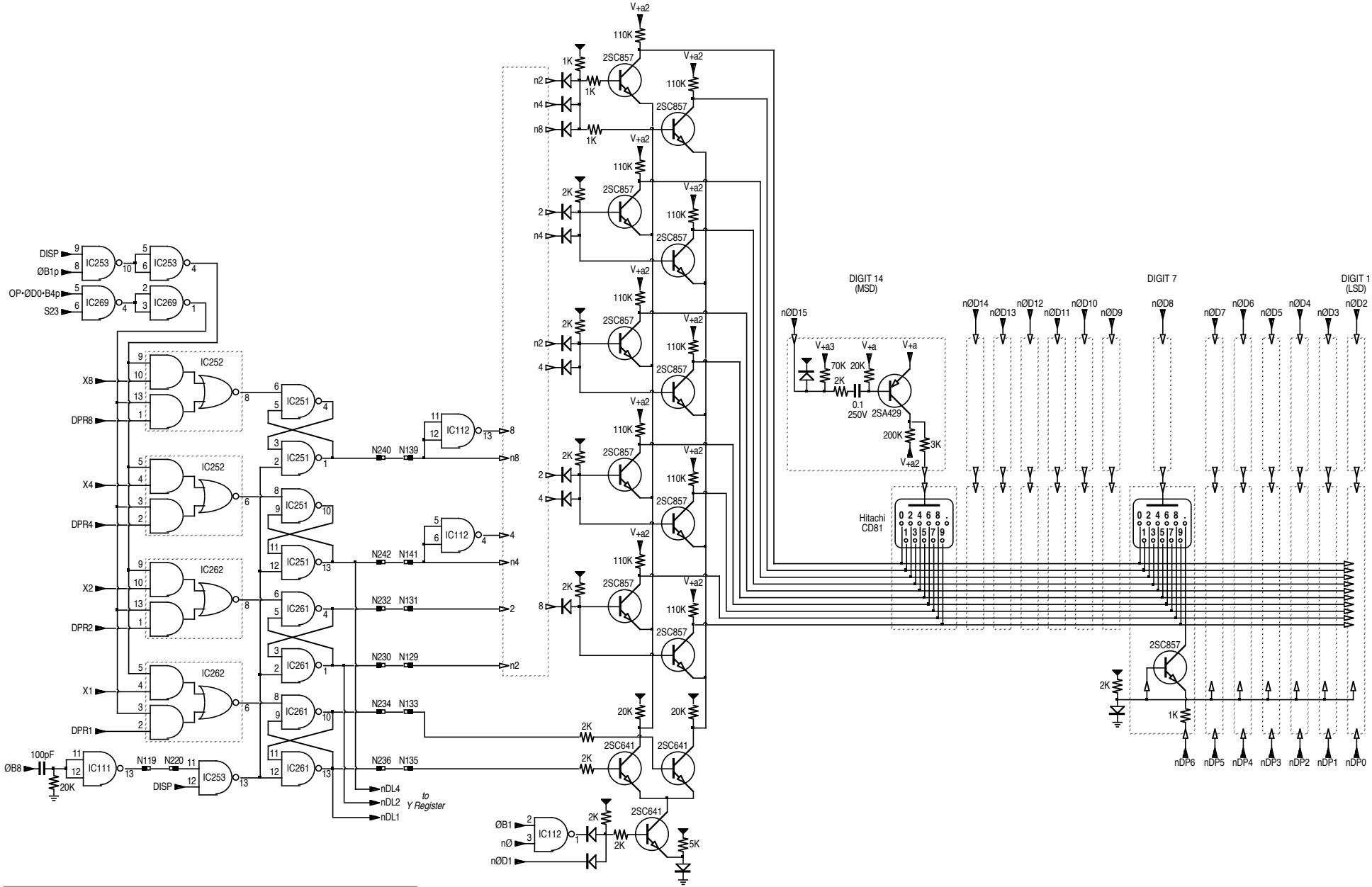

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Section: Display Latch & Display

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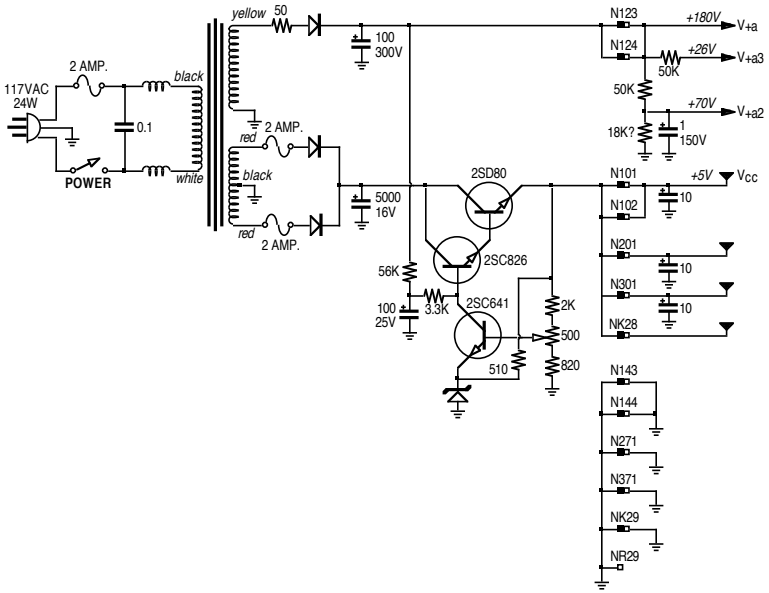
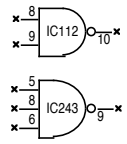


M5304	M5310	M5320	M5330	M5340	M5352	M5373	M5391	M5962
14	14	14	14	14	14	14	14	14
7	7	7	7	7	7	7	7	7
368	310	121	231	111	313	252	142	213	256
388	314	122	237	112	317	262	152	214	266
	326	131	241		318	264		215	268
	336	132	242	221	321	274	211	216	
	337	141	243	229	322		212	217	
	357	151	258	232	324	369	233	218	
	364	161		235	325	379	234	219	
	365	162	316	236	327	387	238		
	374		323	239	328		249	222	
	376	246	335	244	331		267	223	
	383	273	341	245	332		271	224	
	384		351	247	334		272	225	
	385	315	353	248	343			226	
		319	359	251	354		311	227	
		329	361	253	355		312	228	
		333	377	254	360				
		342	378	255	362			281	
		352	380	257	363			282	
		358		259	367			283	
		375		261	370			284	
		386		263	371			285	
				265	372			286	
				269	373			287	
				275	381				
				276	382				
				277	389				
				278					

Unused Gates



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Section: Power Supply

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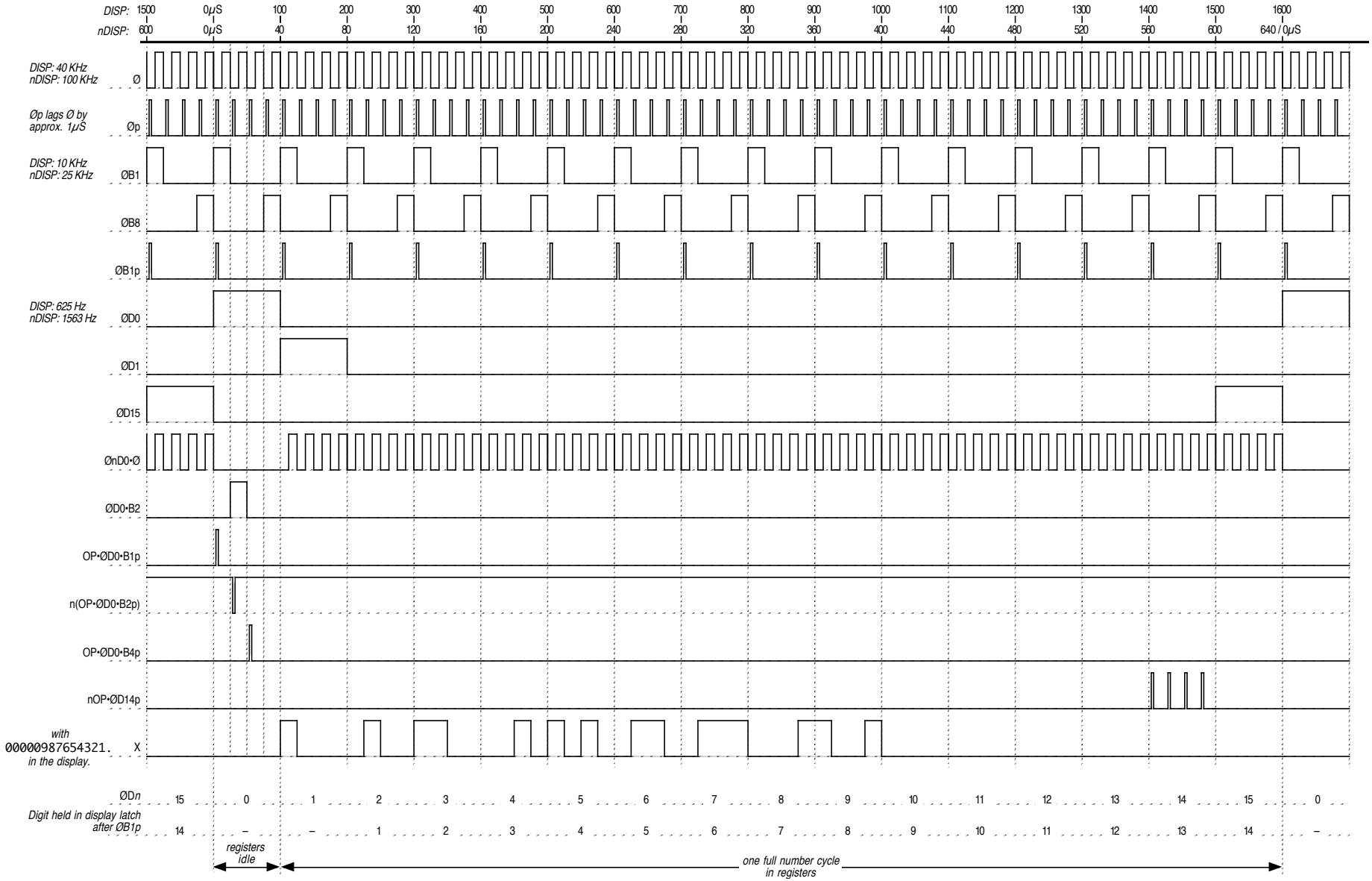
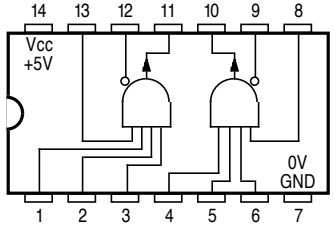
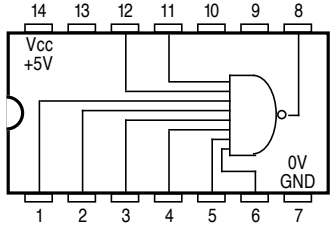


Clock Rates (as measured)
DISP=1 (displaying): 43KHz, 23μS
DISP=0 (calculating): 111KHz, 9μS

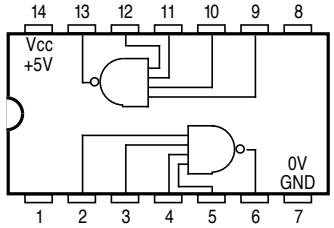
M5304



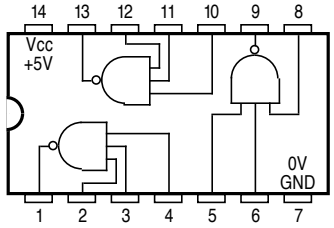
M5310



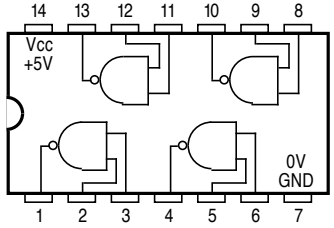
M5320



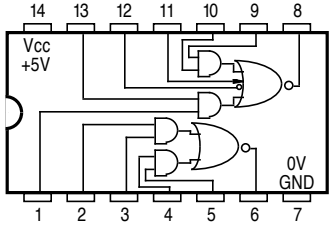
M5330



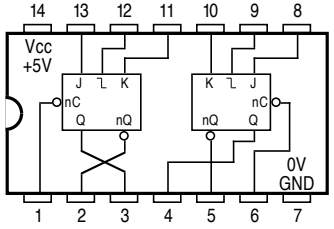
M5340



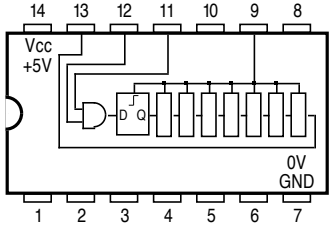
M5352



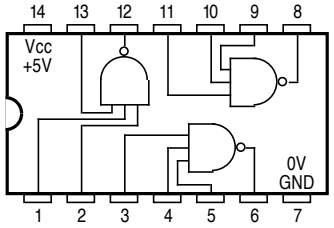
M5373



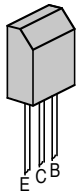
M5391



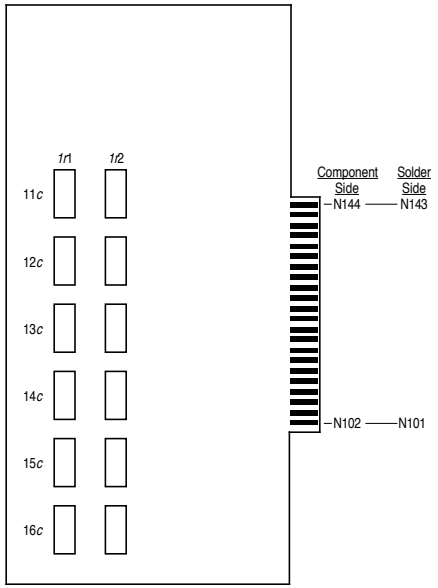
M5962



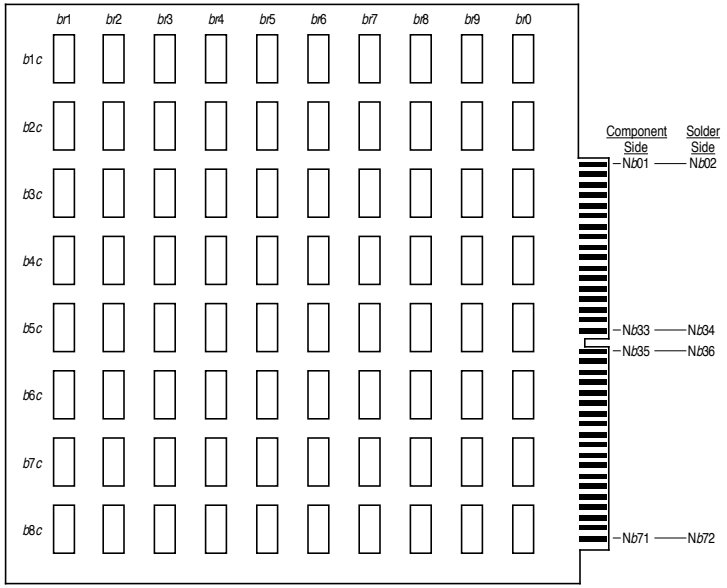
- IC pinouts are derived from the implementation and may not include all connections.
- M5962s are reversed in their orientation on the board relative to all other ICs.



Board 1
(component side view)



Boards 2 and 3
(component side view)



N3

Vcc	1	2	**nP0**
key 8	3	4	DISP
key 9	5	6	*key 0*
key 1	7	8	*key 2*
key 3	9	10	*key 4*
key 5	11	12	*key 6*
key 7	13	14	**KP**
key M+	15	16	nOP
key M–	17	18	nØD15
key ÷	19	20	**K8**
key DP	21	22	**K4**
key Z1	23	24	**K2**
lamp *	25	26	**K1**
key Z2	27	28	***lamp ÷***
key RC	29	30	*key =*
key CE	31	32	*key –*
*key **	33	34	***X Reg IC378-1***
nKCLR	35	36	**CYP**
Z	37	38	**CSTC**
CYS16	39	40	**CSCC**
XØENB	41	42	nOP•ØD14p
Arith IC359-13	43	44	ØD1
CZS10	45	46	***Arith IC360-1***
DPR In	47	48	***X Reg IC370-1***
Arith IC369-10	49	50	nYP1
ØB8	51	52	*switch 5/4*
ØB1	53	54	*Arith IC368-4*
Q-bit IC378-8	55	56	X
X1	57	58	ASUM10
ASUM16	59	60	OP•ØD0•B1p
CYDL, CA54	61	62	DPR
DPGT	63	64	nX=0
n(OP•ØD0•B2p)	65	66	OP•ØD0•B4p
DPNE	67	68	**CQXYD**
CS10S1,S23	69	70	**CZØ**
GND	71	72	**CYØYP**

N2

Vcc	1	2	nP0
nMANUAL	3	4	**nDP0**
DISP	5	6	**nDP6**
nØD0	7	8	**nDP5**
nØD1	9	10	**nDP4**
nKCLR	11	12	**nDP1**
nKP	13	14	**nDP2**
nOP	15	16	**nDP3**
nØD15	17	18	**ØB48**
nØD14	19	20	*D Latch IC253-11*
K8	21	22	**DP>4**
K4	23	24	CZS10
K2	25	26	—
K1	27	28	**DP>3**
Ø	29	30	**nDL2**
Øp	31	32	**DL2**
X Reg IC281-11	33	34	**DL1**
CYP	35	36	**nDL1**
CSTC	37	38	**Z**
CSCC	39	40	**nDL8**
CYS16	41	42	**nDL4**
XØENB	43	44	**ØD1**
Arith XOR1-b	45	46	**nOP•ØD14p**
Arith IC265-6	47	48	*DPR In*
OP•ØD0•B1p	49	50	*X Reg IC272-10*
nYP1	51	52	**ØB8**
Arith IC277-13	53	54	**ØB1**
Q-bit IC246-6	55	56	**OP•ØD0•B4p**
X1	57	58	**X**
CYDL	59	60	**ASUM10**
nX=0	61	62	**ASUM16**
n(OP•ØD0•B2p)	63	64	**DPR**
CZØ	65	66	CQXYD
CS10S1,S23	67	68	***Arith IC263-1***
CYØYP	69	70	**DP>2**
GND	71	72	**DP>6**

N1

Vcc	1	2	Vcc
nDP0	3	4	—
nDP6	5	6	—
nDP5	7	8	**nØD0**
nDP4	9	10	**nØD1**
nDP1	11	12	—
nDP2	13	14	—
nDP3	15	16	ØB1
ØB48	17	18	**nØD15**
nØB8p	19	20	**nØD14**
—	21	22	—
V+a	23	24	V+a
—	25	26	—
ØB8	27	28	—
nDL2	29	30	**Ø**
DL2	31	32	**Øp**
DL1	33	34	—
nDL1	35	36	—
DISP	37	38	—
nDL8	39	40	—
nDL4	41	42	—
GND	43	44	GND

NK (keyboard)

1	***key 1***	17	–	30	***key DP***
2	***key 2***			31	***key ****
3	***key 3***	18	nP0	32	***key /***
4	***key 4***	19	–	33	***key =***
5	***key 5***	20	nDP0	34	***key –***
6	***key 6***	21	nDP2	35	***key RC***
7	***key 7***	22	nDP4	36	**nKCLR**
8	***key 8***	23	nDP6	37	***key CE***
9	***key 9***	24	DP>2	38	***key M+***
10	***key 0***	25	DP>4	39	***key M–***
11	DP>3	26	DP>6	40	***key MR/C***
12	**DPNE**	27	nDP3	41	***key MC/R***
13	**DPGT**	28	Vcc	42	–
14	***switch 5/4***			43	*lamp **
15	CA54	29	GND	44	–
16	–			45	*lamp /*

NR (remote)

1	*key 1*	17	nMANUAL	30	*key DP*
2	*key 2*			31	*key **
3	*key 3*	18	nP0	32	*key /*
4	*key 4*	19	X	33	*key =*
5	*key 5*	20	nDP0	34	*key –*
6	*key 6*	21	nDP2	35	*key RC*
7	*key 7*	22	nDP4	36	nKCLR
8	*key 8*	23	nDP6	37	*key CE*
9	*key 9*	24	DP>2	38	*key M+*
10	*key 0*	25	DP>4	39	*key M–*
11	DP>3	26	DP>6	40	*key MR/C*
12	DPNE	27	nOP	41	*key MC/R*
13	DPGT	28	nDP3	42	ASUM16
14	*switch 5/4*			43	XØENB
15	CA54	29	GND	44	Ø
16	—			45	nØD0

Facit 1123 Calculator

Section: Connectors
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- Italicised expressions are connections with no signal name in the schematic.
- Bold-faced expressions are signal sources.
- See preceding page for connector orientation.